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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,802	12/22/2000	Michihide Kimura	1448.1007	9060

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,802	KIMURA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,13-18,20-22 and 24-28* is/are pending in the application.

4a) Of the above claim(s) *7-12, 19,23,29-31* is/are withdrawn from consideration.

5)☒ Claim(s) *13-18,20-22 and 24-28* is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/03, 12/22/00*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Clams 7-12 and clams 19,23,29-31 have been canceled. Clams 1-6,13-18, 20-22,24-28 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hartnett et al. (6,167,4:9) in view of Kim (6,343,353).

3. As to claims 1 ,4, Hartnett disclosed a processing apparatus (see fig.6) as claimed comprising at least :

a) a control unit microcontroller (178) for processing an operation instruction (see e.g. the expanded-cycle instruction) as a specific application-purpose operation (e.g. see the microcode controller controlling the instruction execution in col.9, lines 1-23, see also col.7, lines 39-55, col.8, lines 1-13 for the microcode controller during the extended cycles);

b) a specific application-purpose instruction operating unit (e.g. fig.6 (12) IP, see also fig.6) for supporting a flexible pipeline structure (see the pipeline processing in col.8, lines 27-43) and capable of being designed to carry out an operation (e.g. address generation) of the specific application-purpose instruction for each application field

subsection) (see the address generation for the corresponding subsection in *1.8, lines 27-40, see col.6, lines 59-67 for background, the extended cycle instruction added more delays cycles, see col.7. lines 56-66).

4. Hartnett did not specifically show the writable register prescribing the number of cycles from the instruction was issued to when the instruction become possible to issue as claimed. Although Hartnett prescribed a number of cycles (see the 2y , Ix and E cycles) when the instruction was issued to when the result was provided (see the number of cycles from the reading of the memory to the execution cycle 2x in col.6, lines 59-67, col.7, lines 56-67), Hartnett did not specifically show the writable register for prescribing the number of cycle. No hardware was shown to store the number of cycles. However, Kim disclosed a writable register for storing prescribed number of cycle (see the wait register for storing the extended cycles in 3, lines 51-67, col.4, lines 4-9, lines 51-67, col.5, lines 1-32, see also fij.6,8 for the extended cycle). It would have been obvious to one of ordinary skill in the art o sue Kim in Hartnett for include the writable register prescribing or storing the number of cycle as claimed because the use of Kim could provide Hartnett the control capability to save a predefined set of cycle number into a configurable storage for a subsequent issue of the instruction , thereby increasing the flexibility of the instruction timing based on the value stored in the writable register , and it could be readily achieved by installing the writable register of Kim with modified access parameters (e.g. such as the register width, R/W pods) into Hartnett so that the writable register of Kim could be recognized by Hartnett in order to achieve the enhanced flexibility of the instruction sequence, and because Hartnett

already taught the use of the extension of the number of cycle in the instruction sequence, one of ordinary skill in the art should be able to recognize the need of a storage of a given format, such as a register, buffer , or memory location, for designating the extended cycle number, and for the above reasons , provided a motivation.

5. As to the specific application purpose instruction, Hartnett's standard and non-standard instructions are applicable as specific application purpose instructions because they were directed to the program executed in a simulation system (e.g. see col.1 , lines 14-26). Simulation is a specific application purpose operation.

6. As to the latest amended feature of issuing of an immediate subsequent instruction same as the instruction of the specific application-purpose instruction operation unit, Hartnett also taught the issuing of immediate instruction which the same as the specific instruction (see the instruction cycle of subsequent instruction N+1 in fig.3).

7. As to claim 2, the specific application-purpose instruction unit of Hartnett was an IP as well (see fig.l (12 IP)).

8. As to claim 3, Hartnett's control unit microcode controller) and the specific application-purpose instruction unit were within the core processor (e.g. see fig.6 (12), see also fig.l I12j, col.6, lines 3-13 for the IP unit for executing and control the instructions).

9. As to claim 4, As to the "result" provided in the claim , Hartnett 's result must

be provided before the start of 2x cycle, otherwise the number of cycles would have been extended continually.

10. As to claim 5, Hartnett also prescribed the number of cycle from when the issue of an instruction (the first instruction in the interrupt handler) to when it became possible to issue an immediately subsequent instructions same as the specific application purpose instruction (see the fetch of the original instruction at MX+x+1 cycle after the fetch of the fist instruction in col.16, lines 1-2, col.17, lines 1-16).

11. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further taught the features of the change of flag between the number of cycles from the issue of the instruction to the possible issue of same instructions in succession, and become the same as another number of cycles which was from the instruction was issued to the possible use of the result, and the possible issue of the same instruction in succession in each cycle based on the flag.

12. Claim 17 is allowable over the art of record for reciting the combined features of the storage of the context after the execution of a program has interrupted, the storage of a value in register or a flag indicating that instruction address, which ahs interrupted the execution , is to detect the operation exception that occurred during the execution of the specific application purpose operation instruction, confirmation of the operation state indicating the detection which occur during the execution of the specific

purpose instruction by referring the content of the register or the flag, the carrying out of the exception according to the confirmation , and return from interruption.

13. Claims 20-22 are allowable over the art of record . None of the prior art or record teaches combined features of

a) the exception detection flags, the specific application purpose instruction execution setting the valid operation exception sate , notification of the interrupt control due to the of instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag invalidating instruction and invalidation the exception detection flag (claim 20),

b) the exception detection flags, the specific application purpose instruction execution setting the valid sate , notification of the interrupt control due to the operation exception of the instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag read instruction (claim 21) ;

c) the execution setting the valid sate , notification of the interrupt control due to the exception detection flags, the specific application purpose instruction operation exception of the instruction when the flag was set to valid state during the trap to generate the interruption and the exception detection flag write instruction (claim 22) .

14. Claims 24-28 are allowable over the art of record for reciting the combined features of the condition code register and the branch/interrupt return instruction control unit for determining the interrupt generation based on the value held in the condition code register and the value in the instruction field during the execution of the trap instruction, and the notification that the interrupt is to be generated.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Hobbs et al. (5,197,138) is cited for the teaching of the detection of exception (see col.11, lines 27-66).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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